

PRIOR ART

FIG. 1

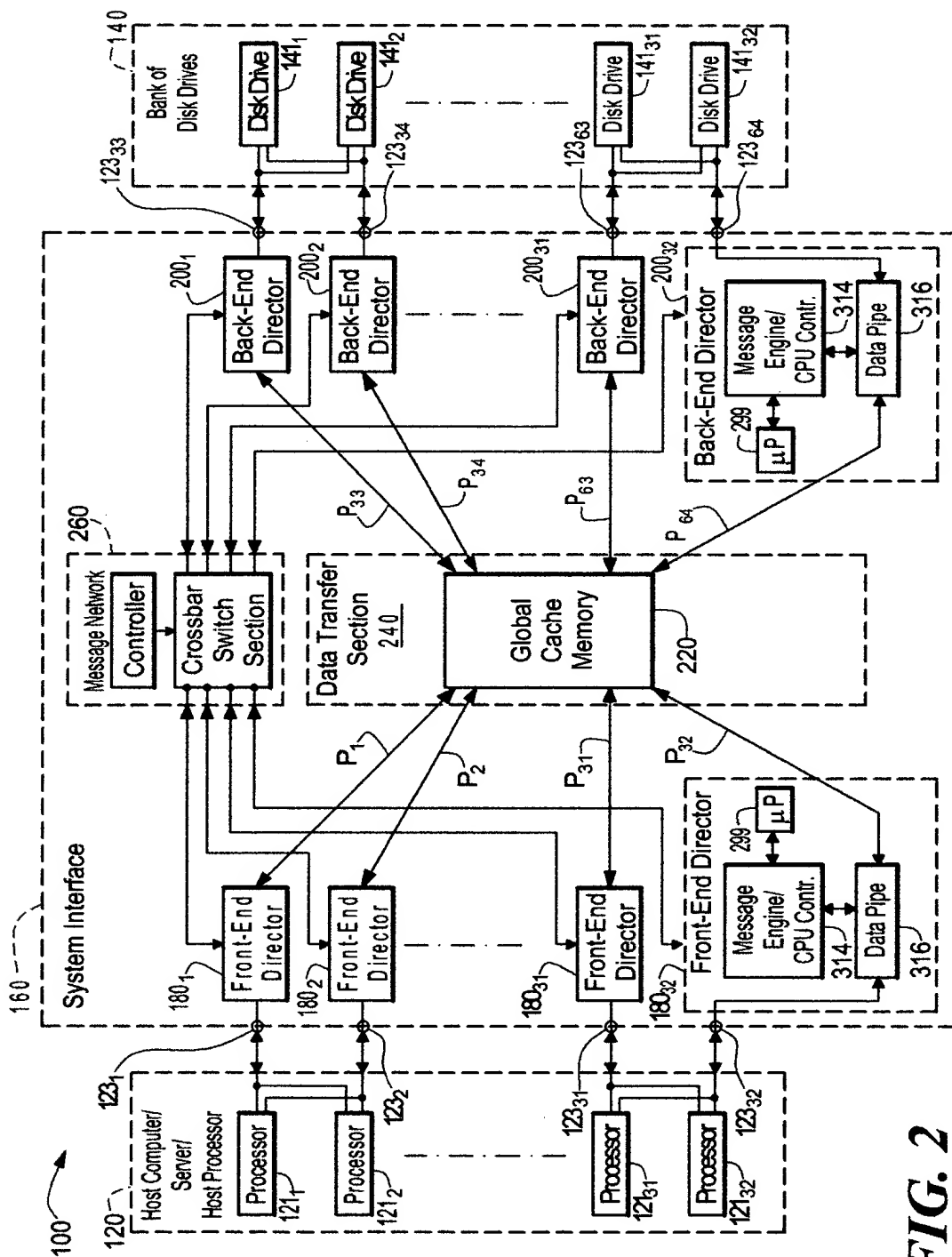
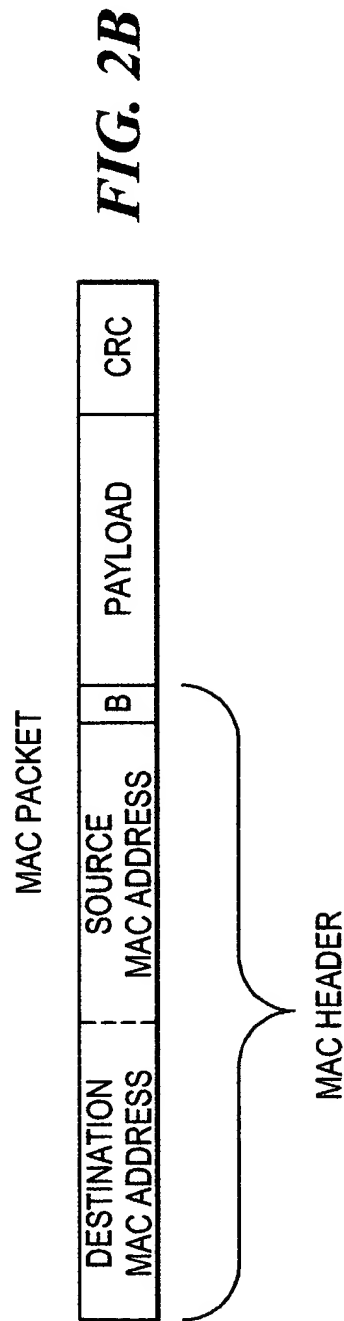
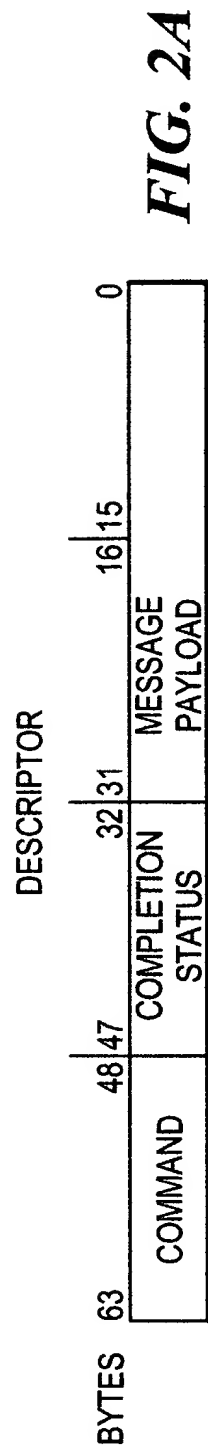


FIG. 2





Serial No.: 09/606,730

4/25

FIG. 3

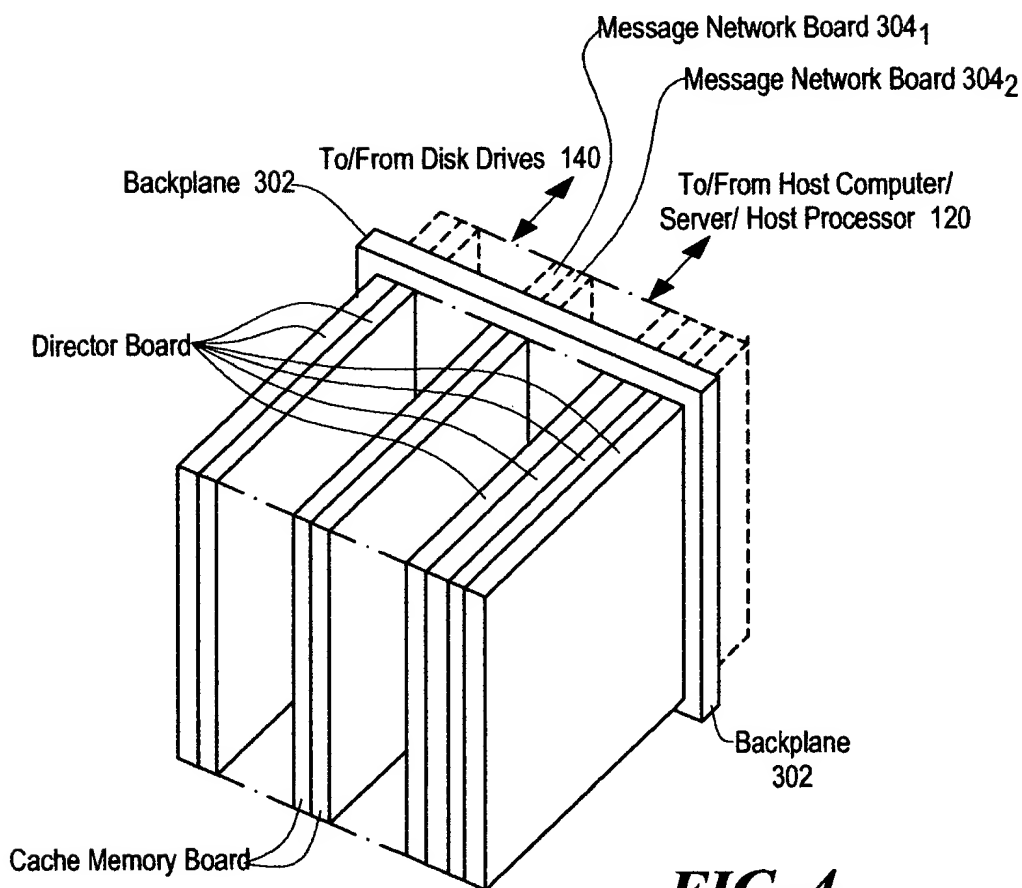
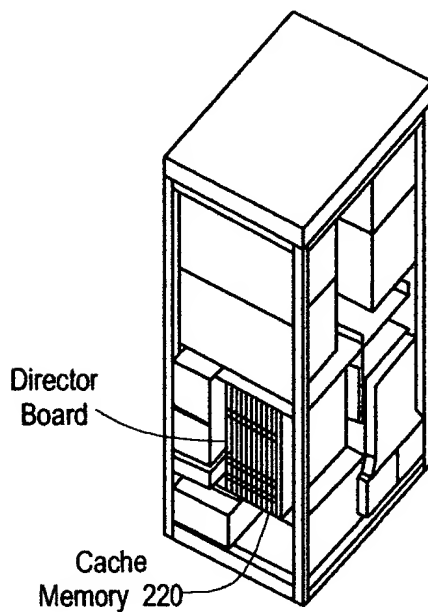
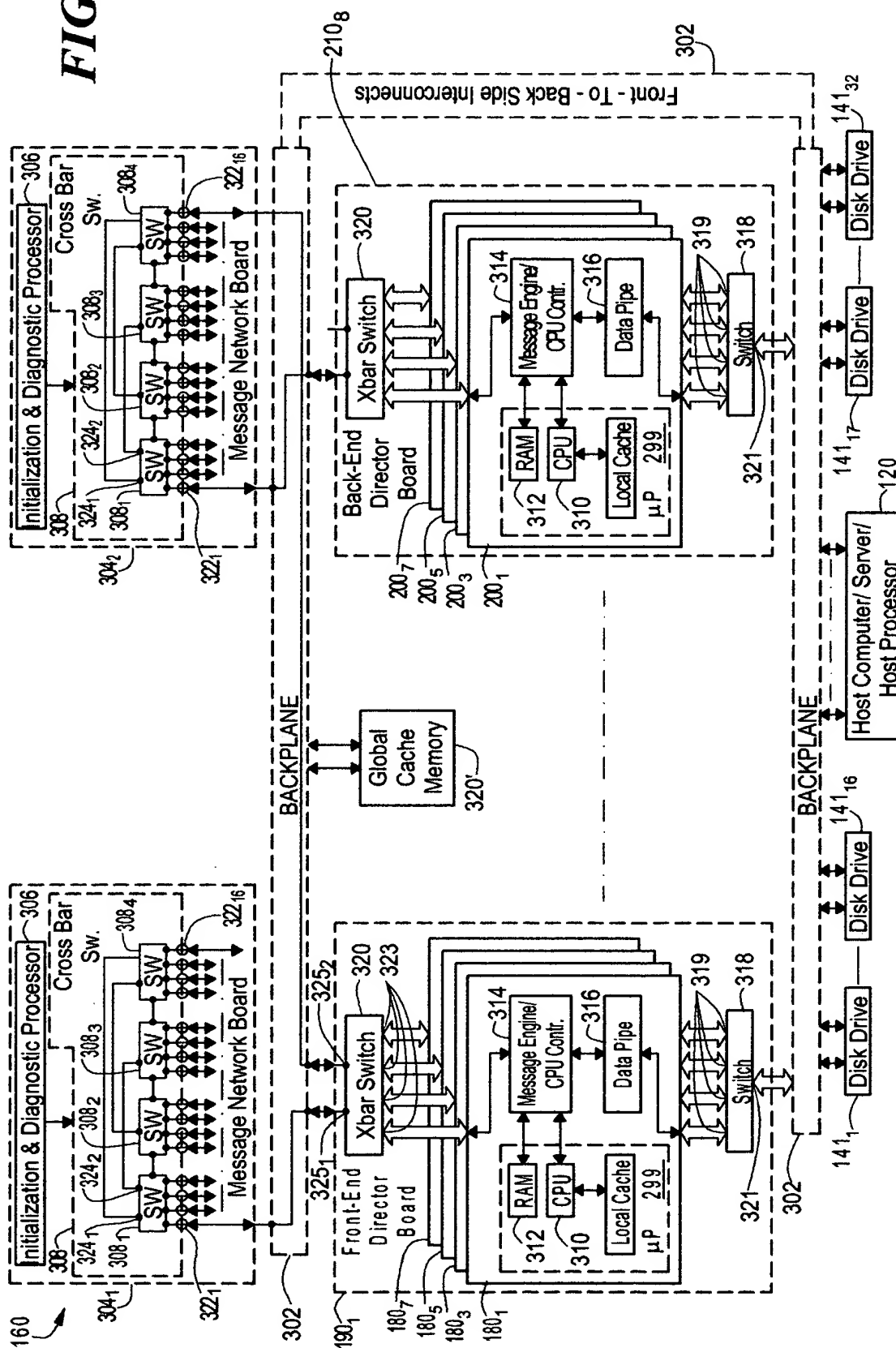
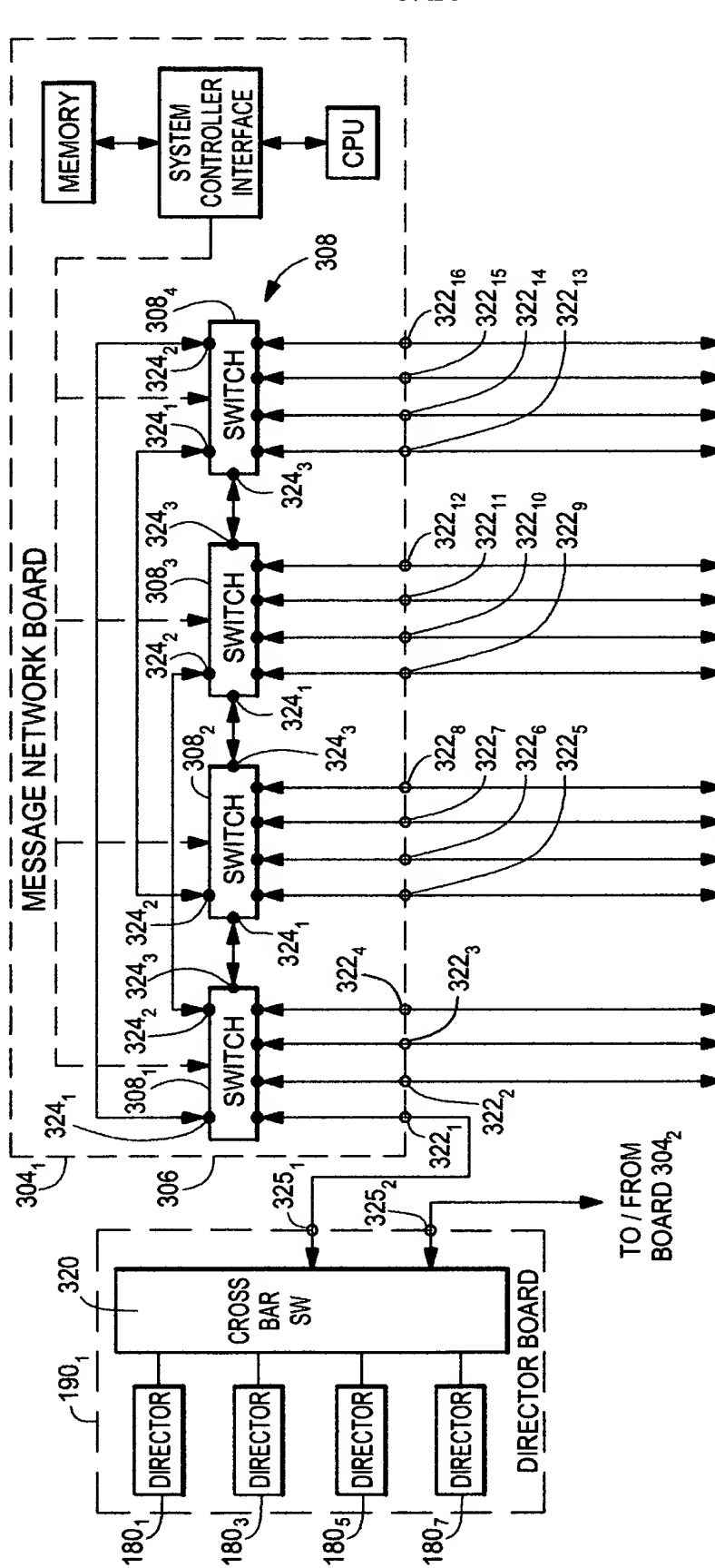


FIG. 4

FIG. 5





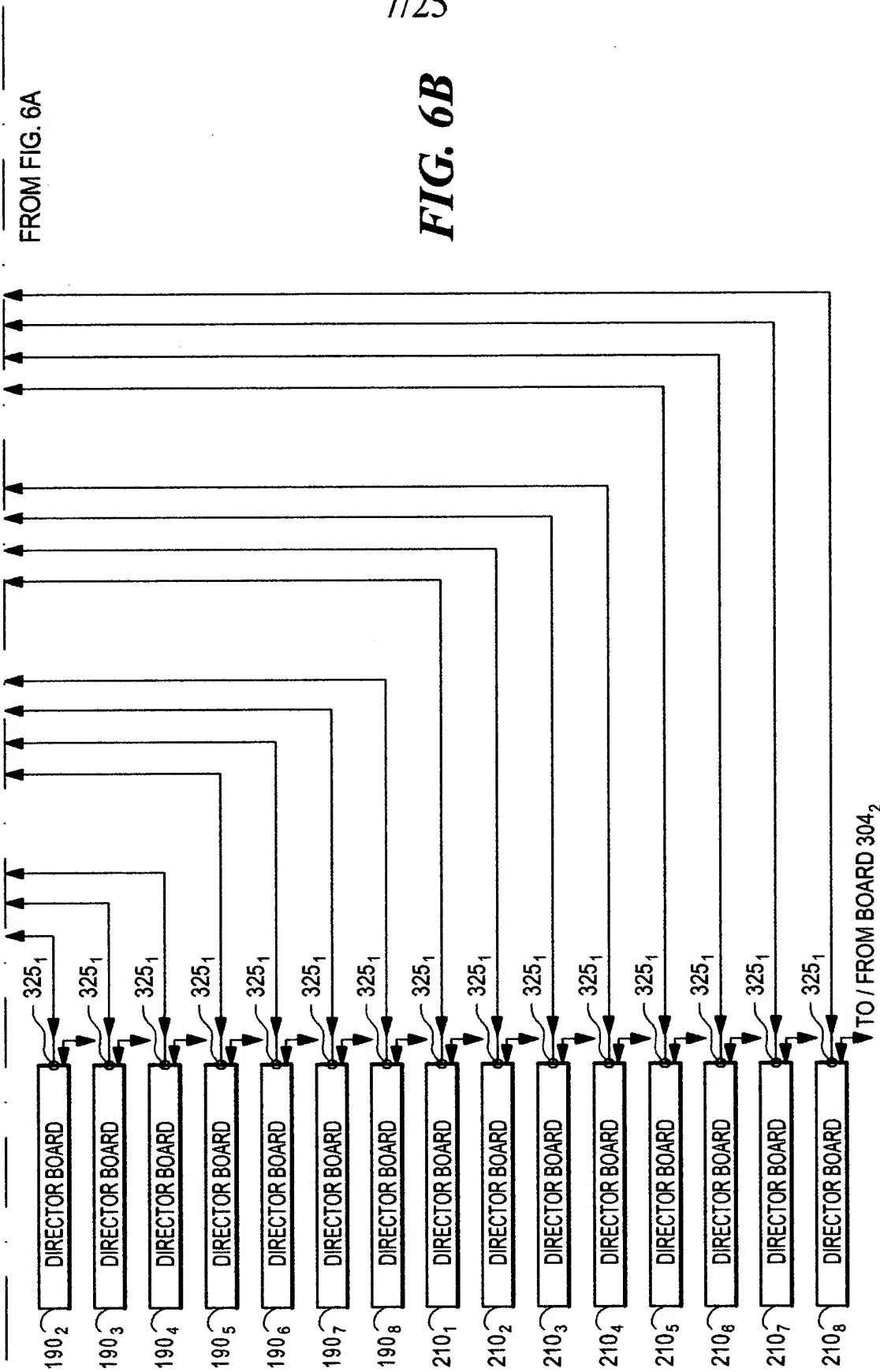
TO FIG. 6B

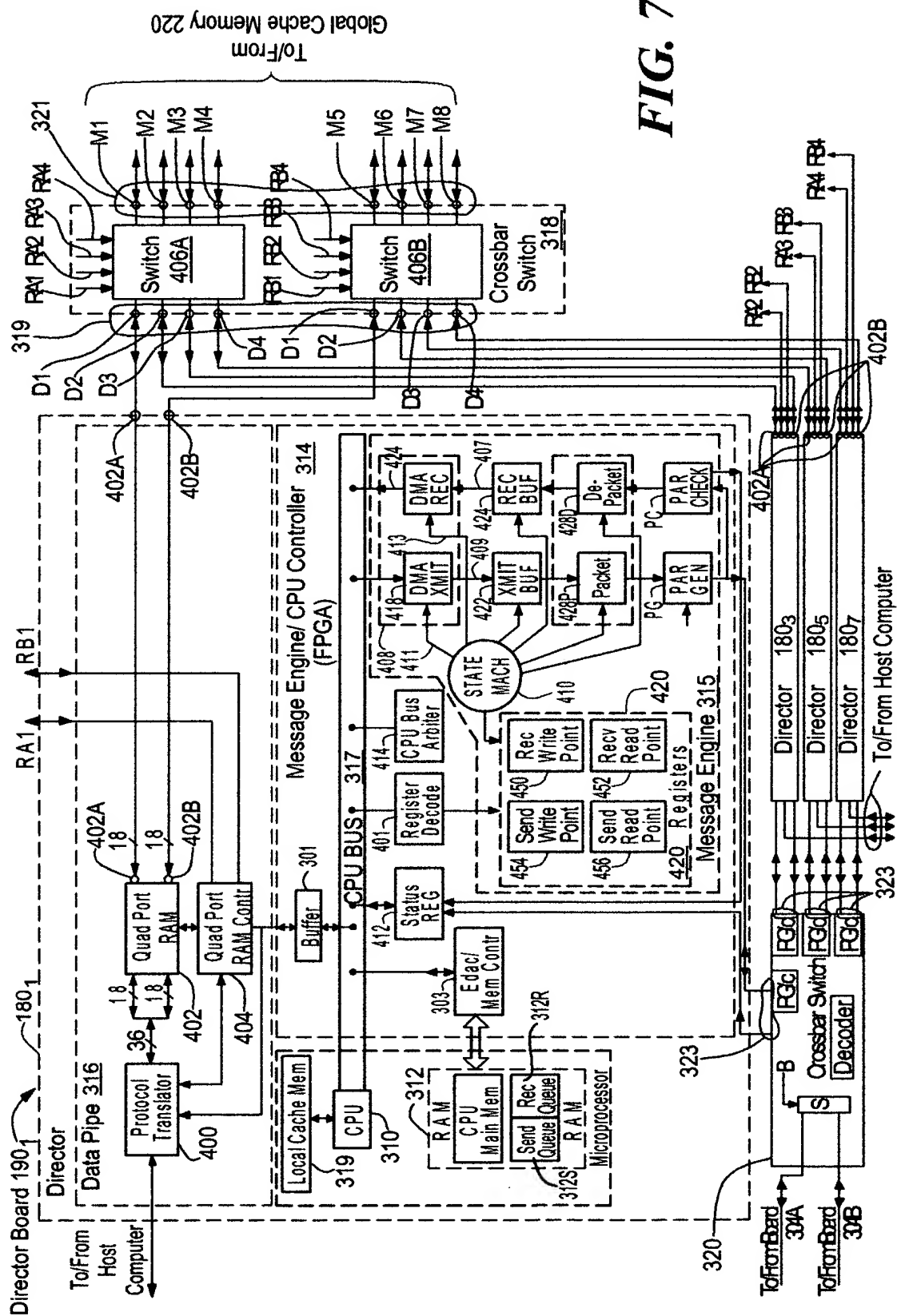
FIG. 6A

FIG. 6
 FIG. 6A
 FIG. 6B



Serial No.: 09/606,730
7/25







Serial No.: 09/606,730

9/25

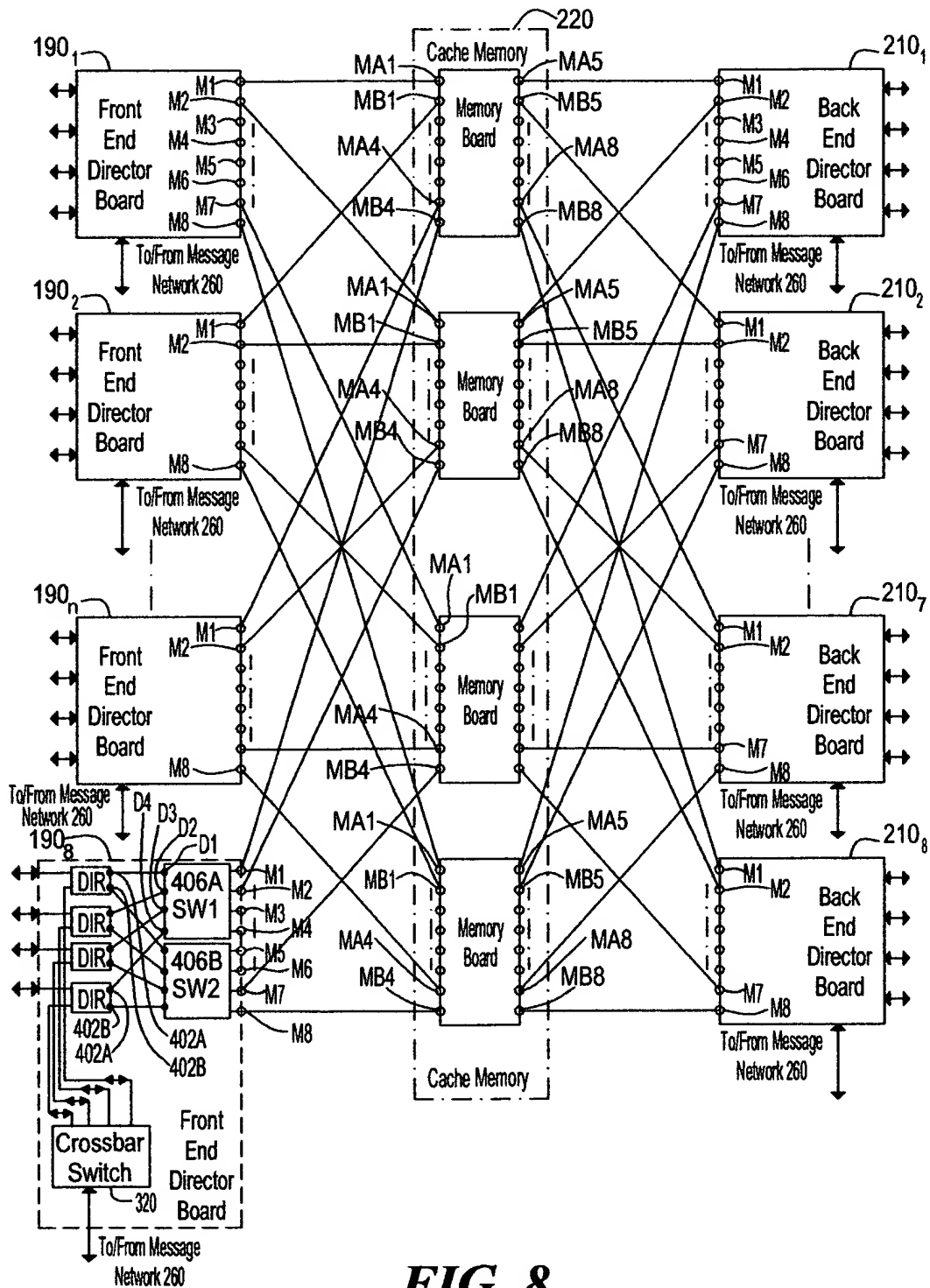


FIG. 8

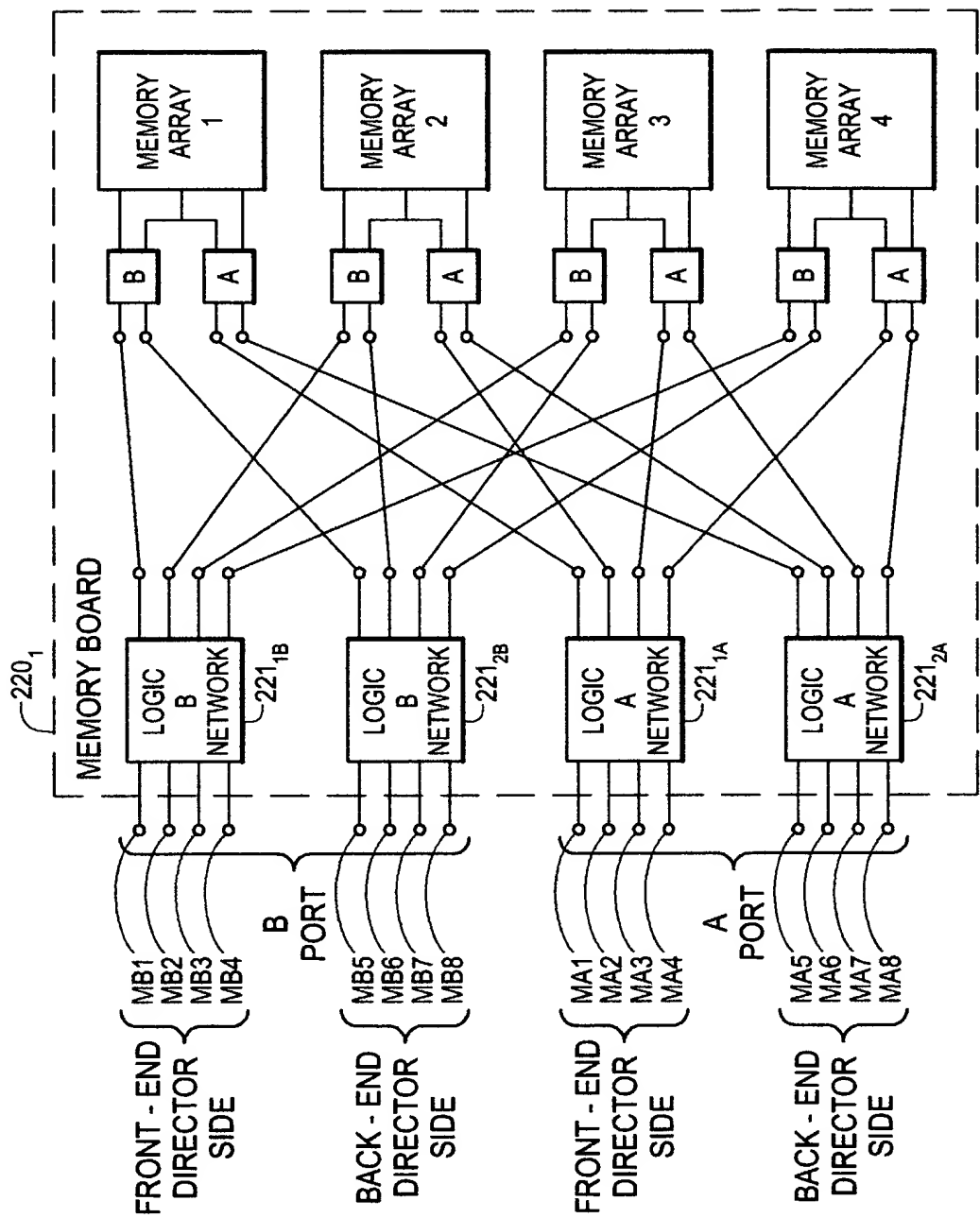


FIG. 8A

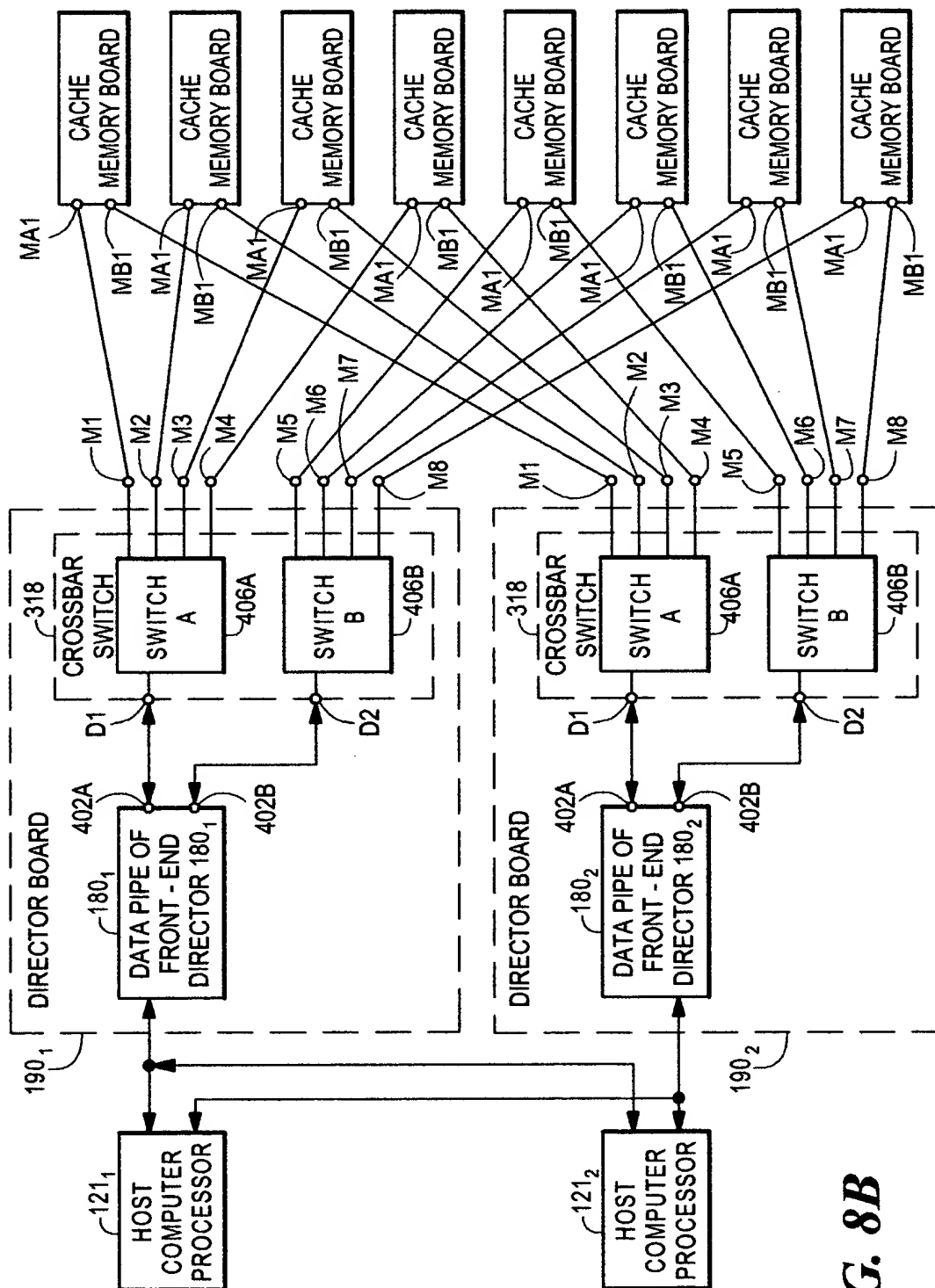


FIG. 8B

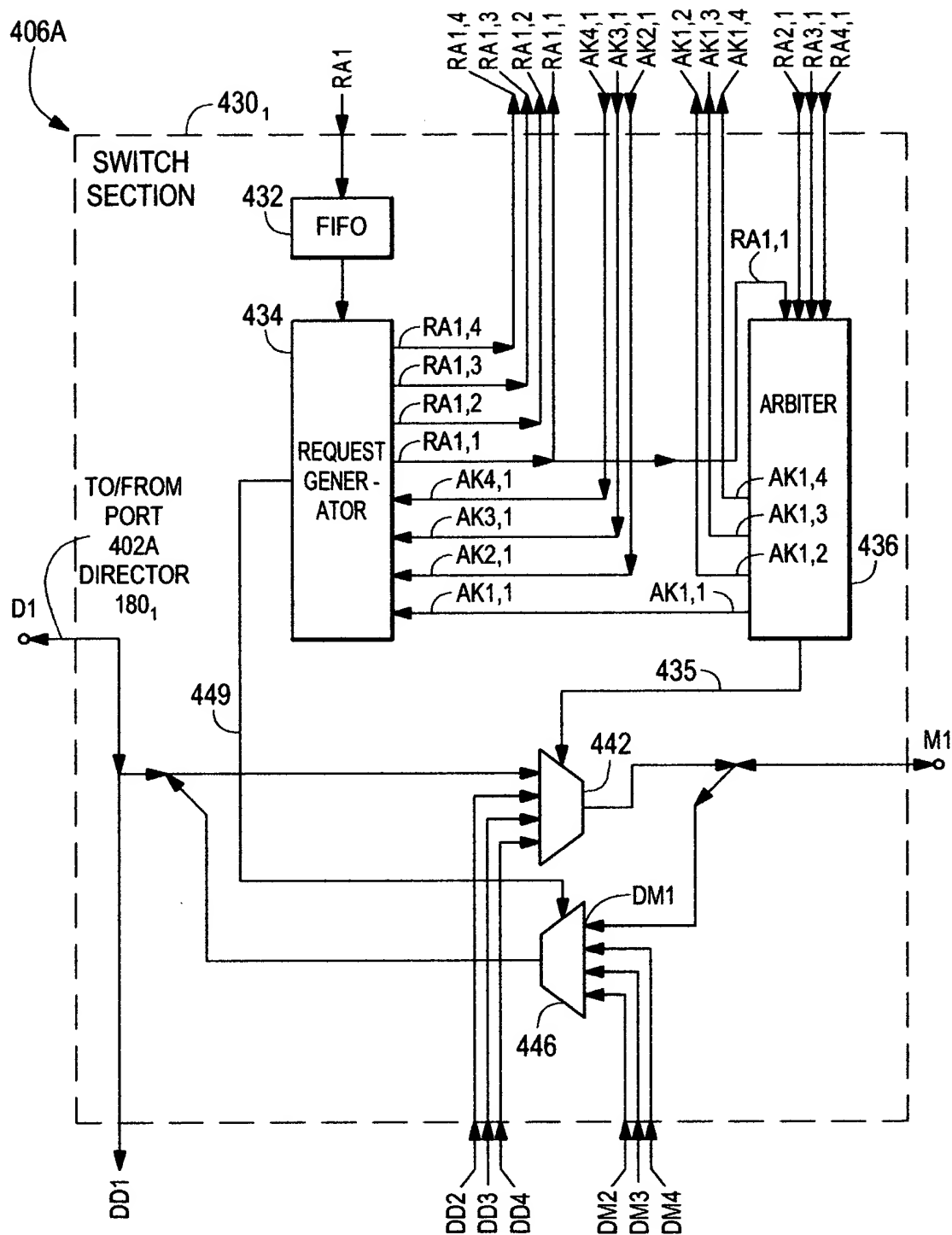


FIG. 8C

FIG. 8C-1

FIG. 8C-2

FIG. 8C-1

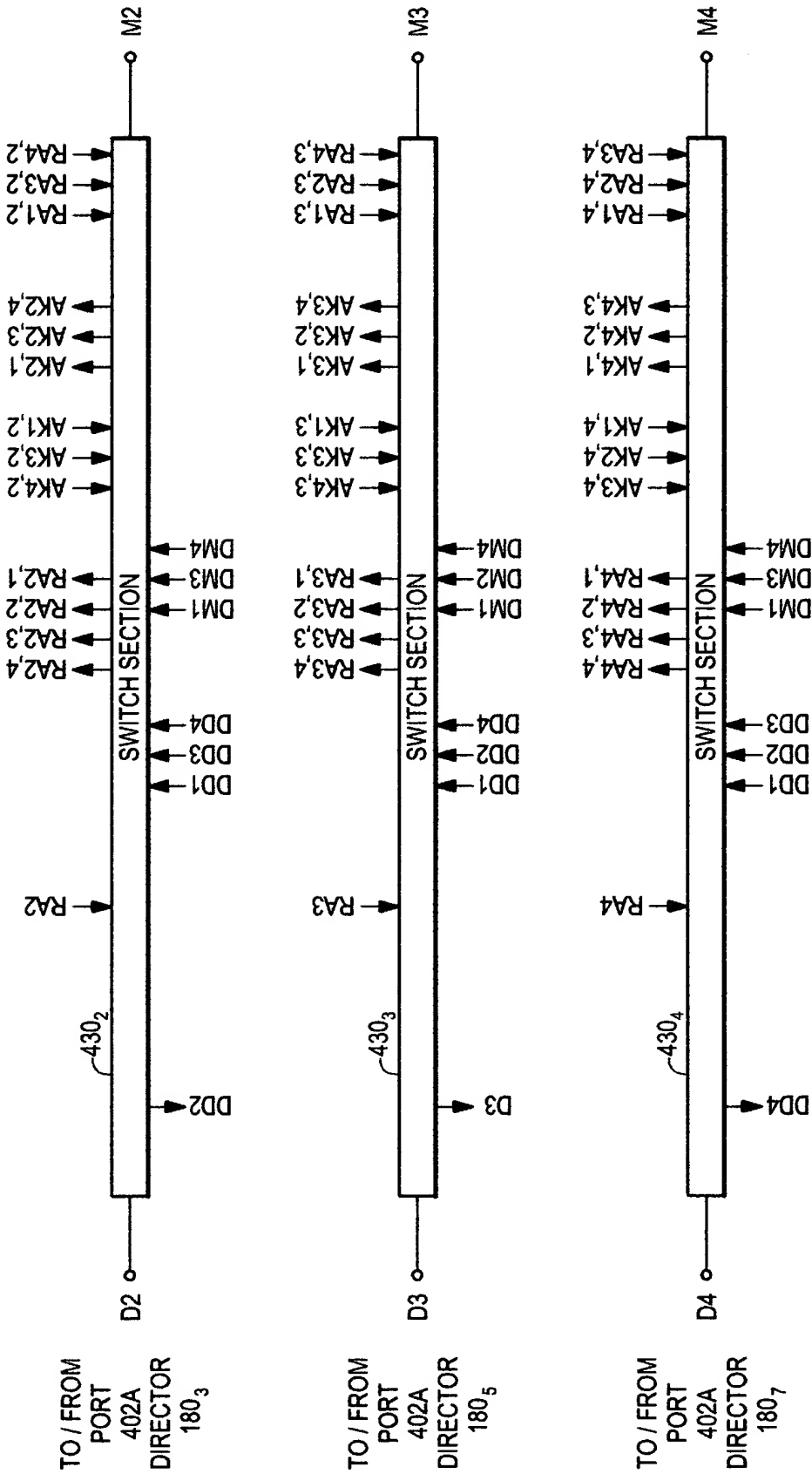


FIG. 8C-2

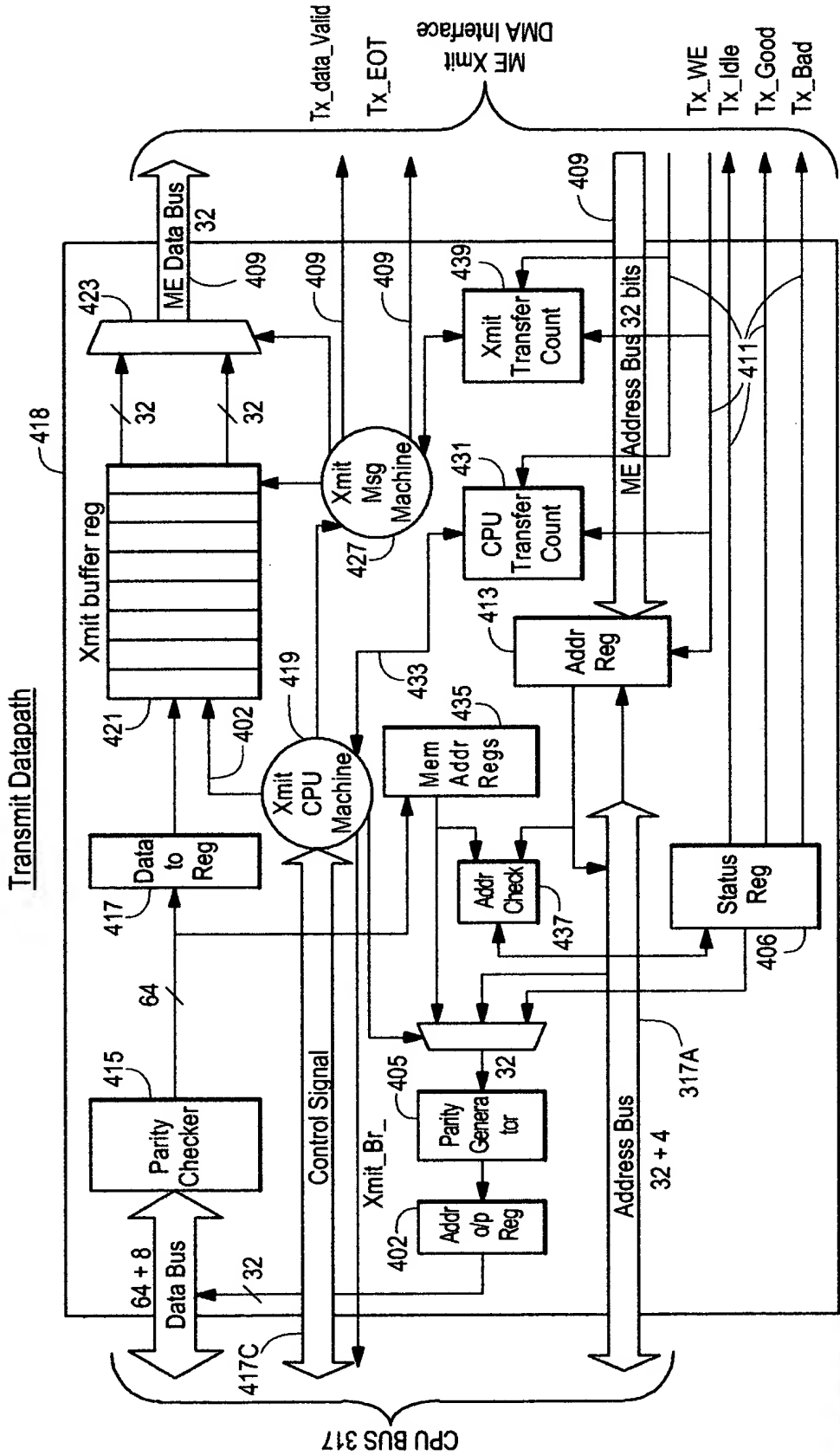


FIG. 9

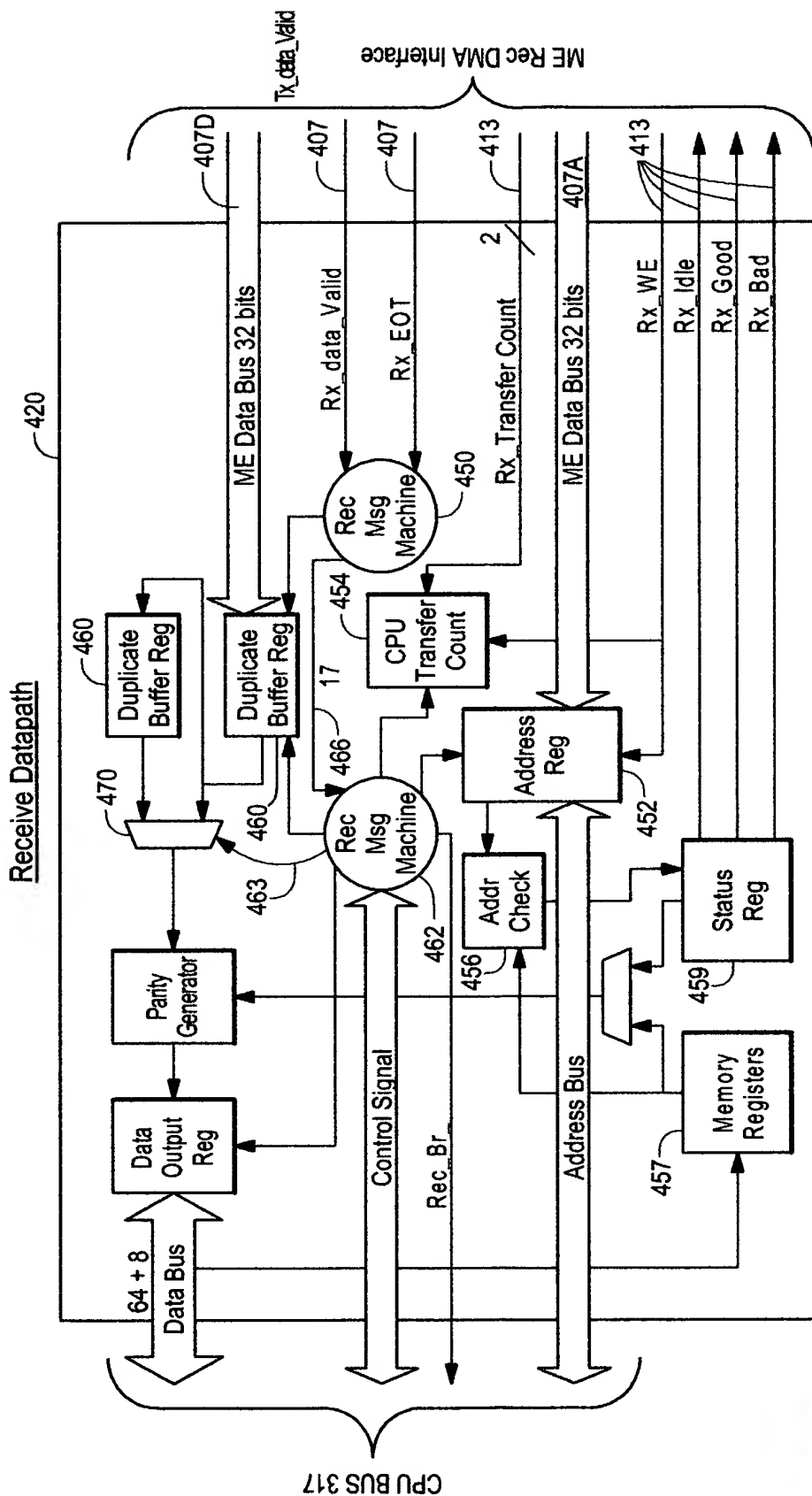


FIG. 10

FIG. 11

FIG. 11A

FIG. 11B

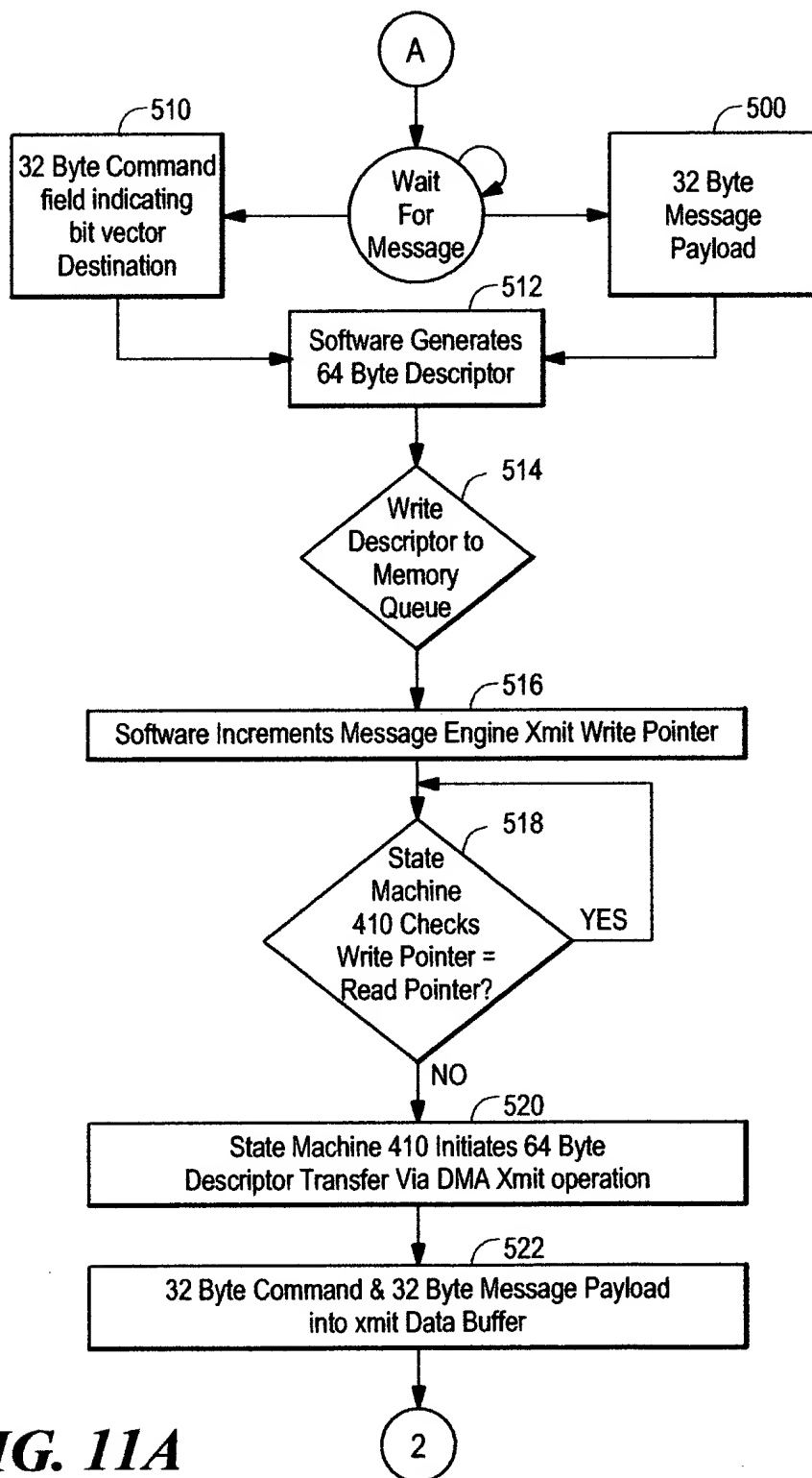


FIG. 11A



Serial No.: 09/606,730

17/25

Message Bus Send Operation Continued

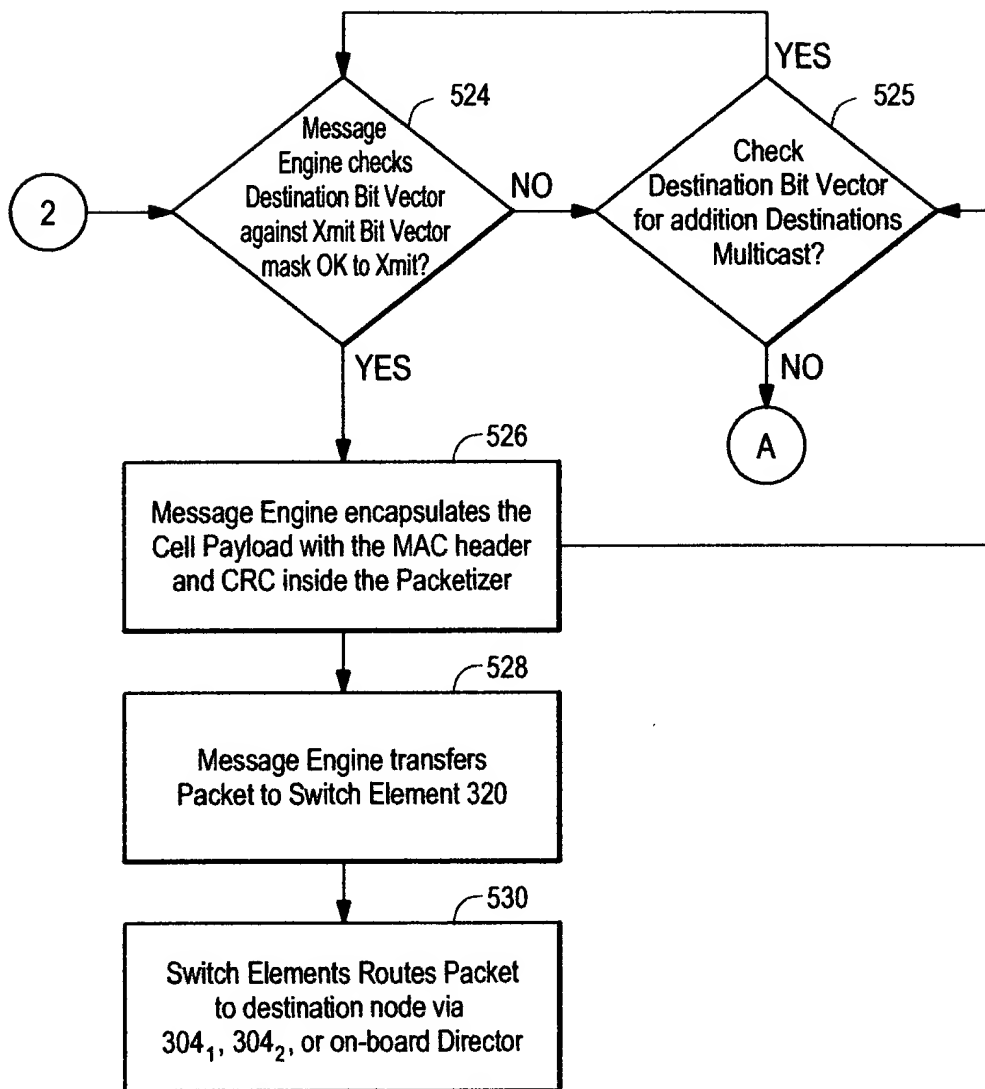
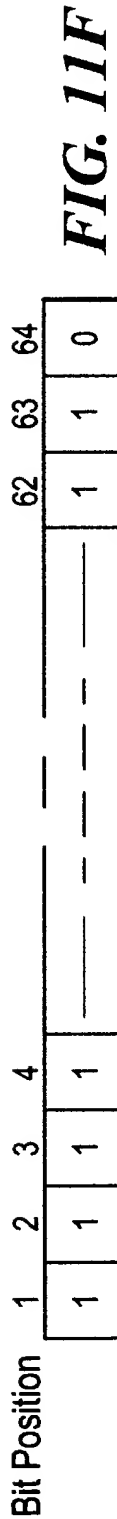
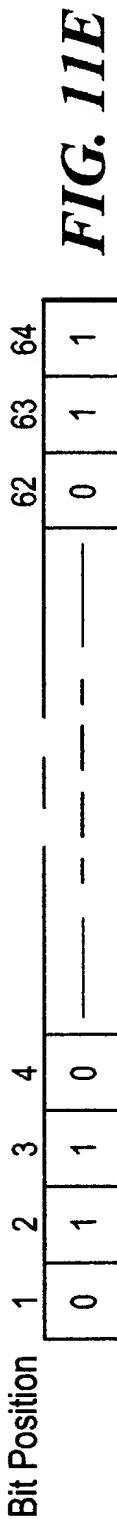


FIG. 11B





Serial No.: 09/606,730

19/25

FIG. 12

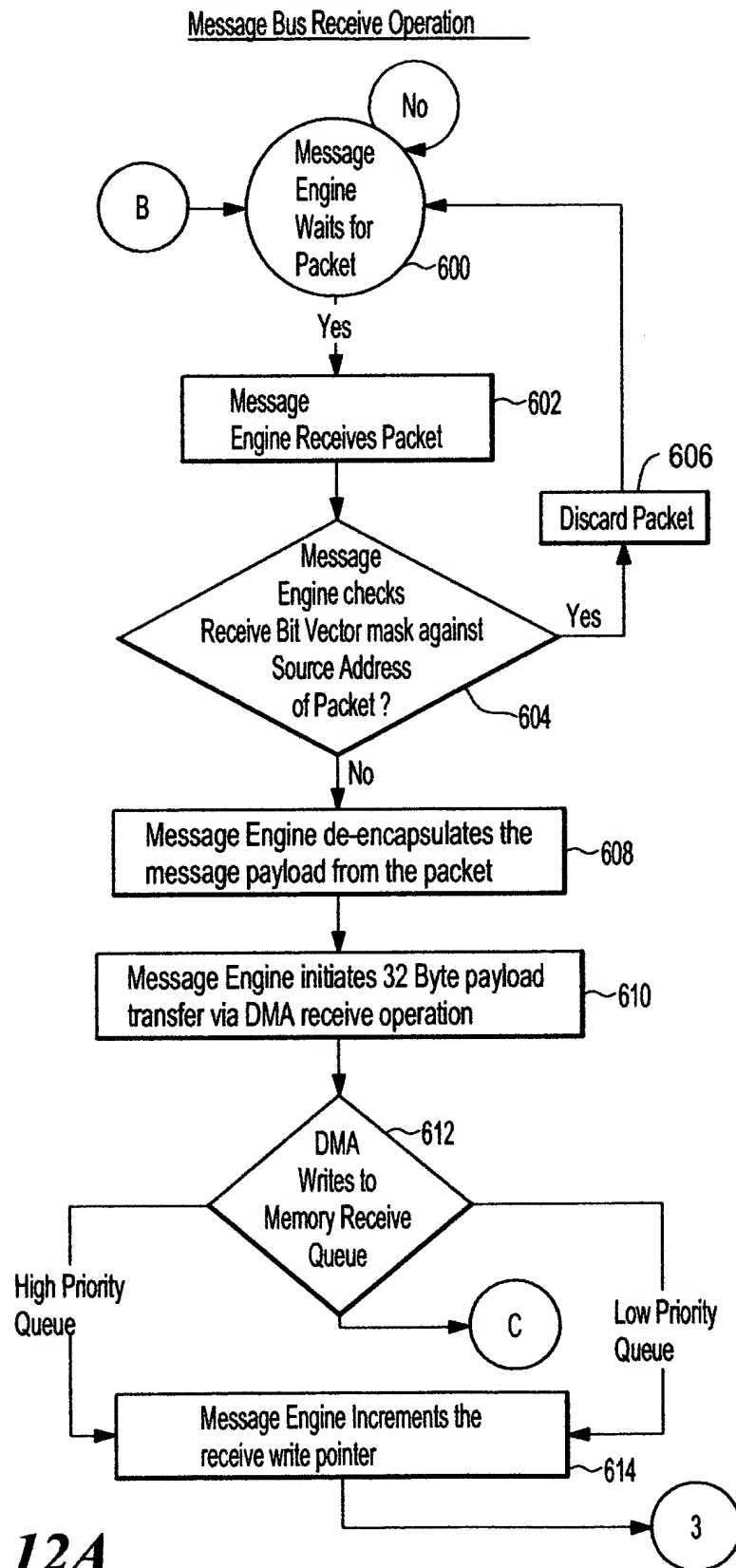
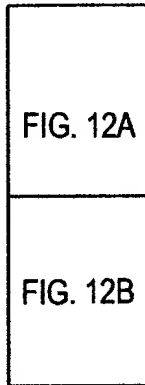


FIG. 12A



Serial No.: 09/606,730

20/25

Message Bus Receive Operation Continued

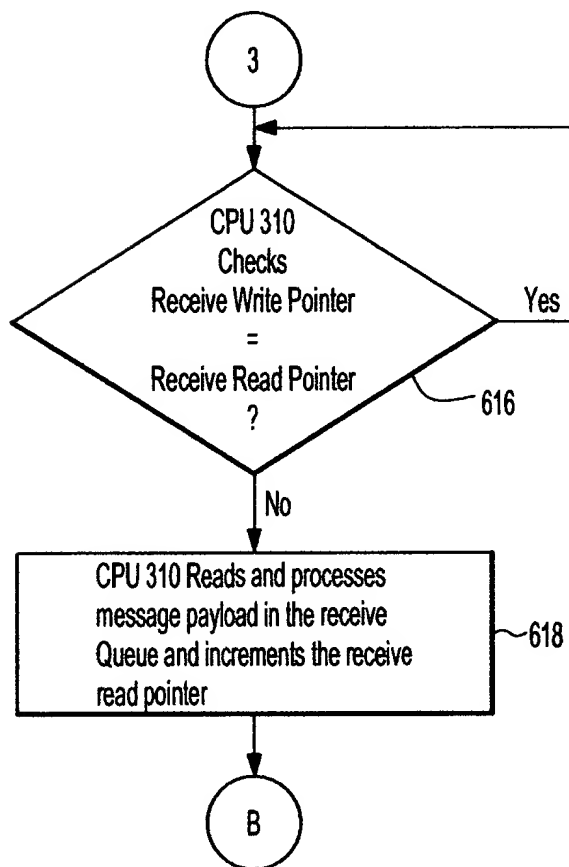


FIG. 12B

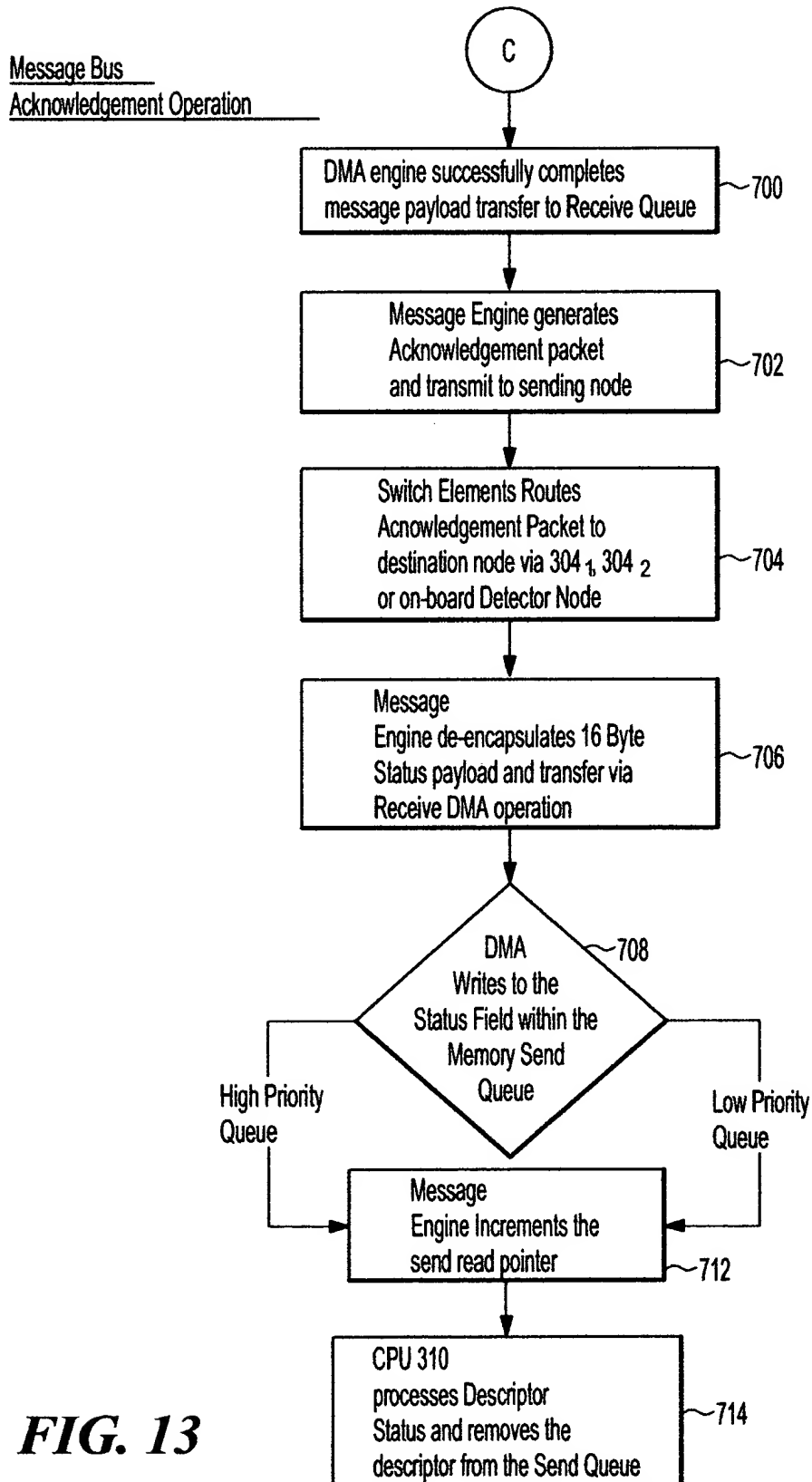


FIG. 13

Xmit CPU flow

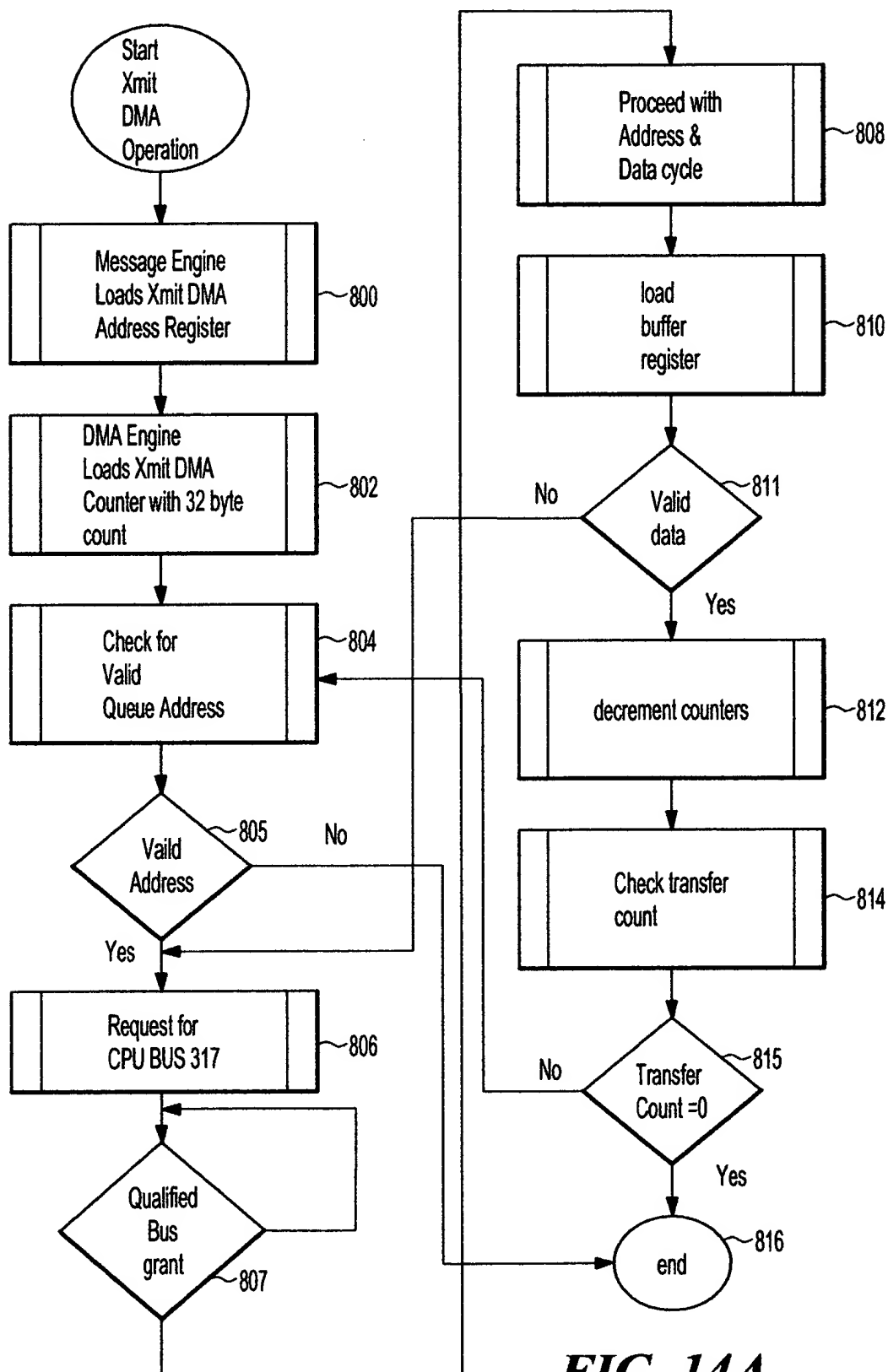


FIG. 14A



Serial No.: 09/606,730

23/25

Xmit Msg flow

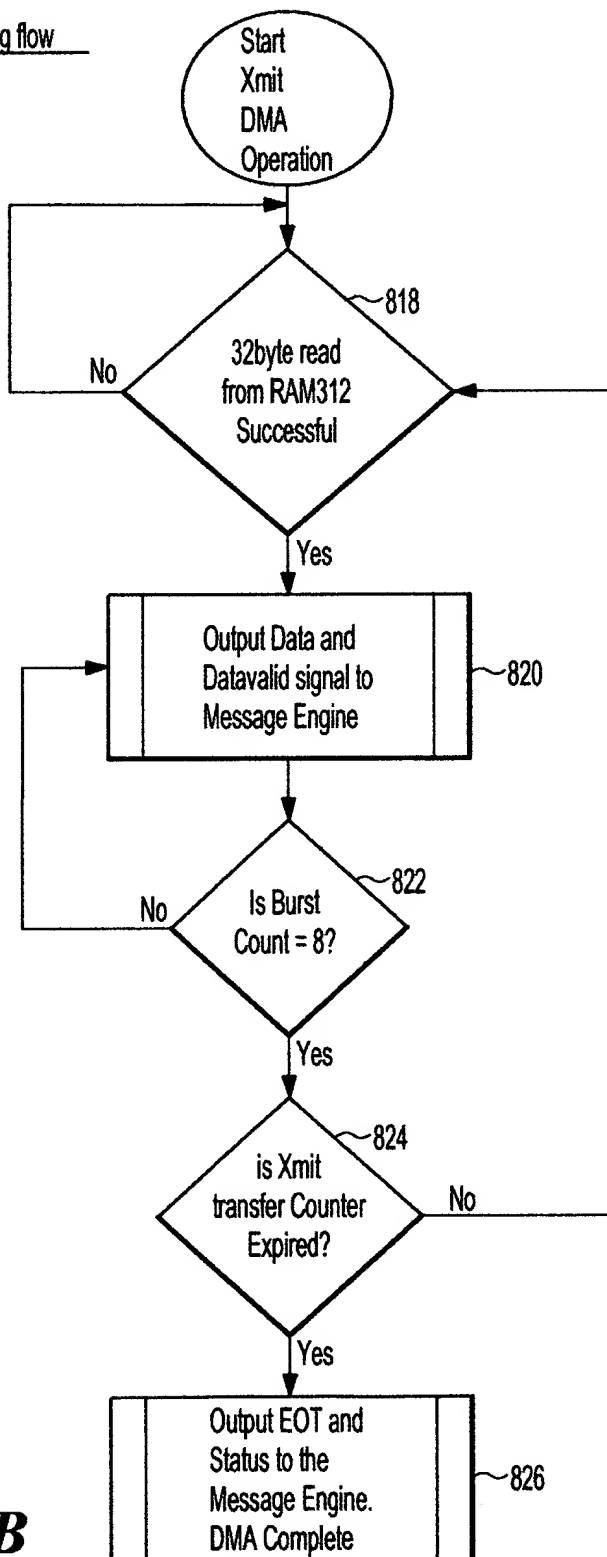


FIG. 14B



Serial No.: 09/606,730

24/25

Rec msg flow

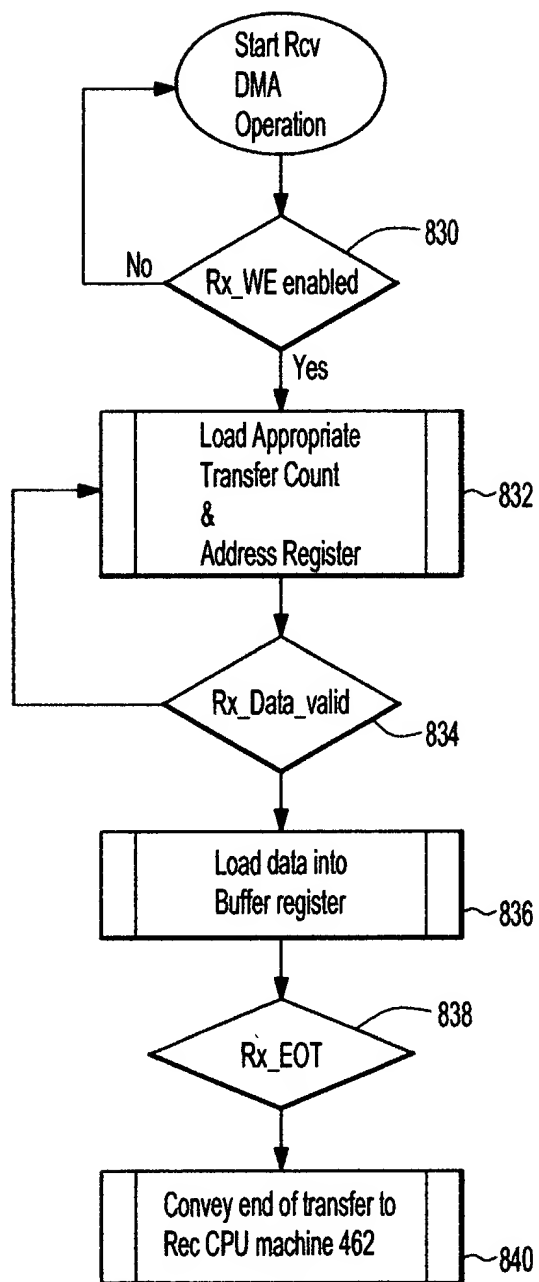


FIG. 15A

Rec cpu flow

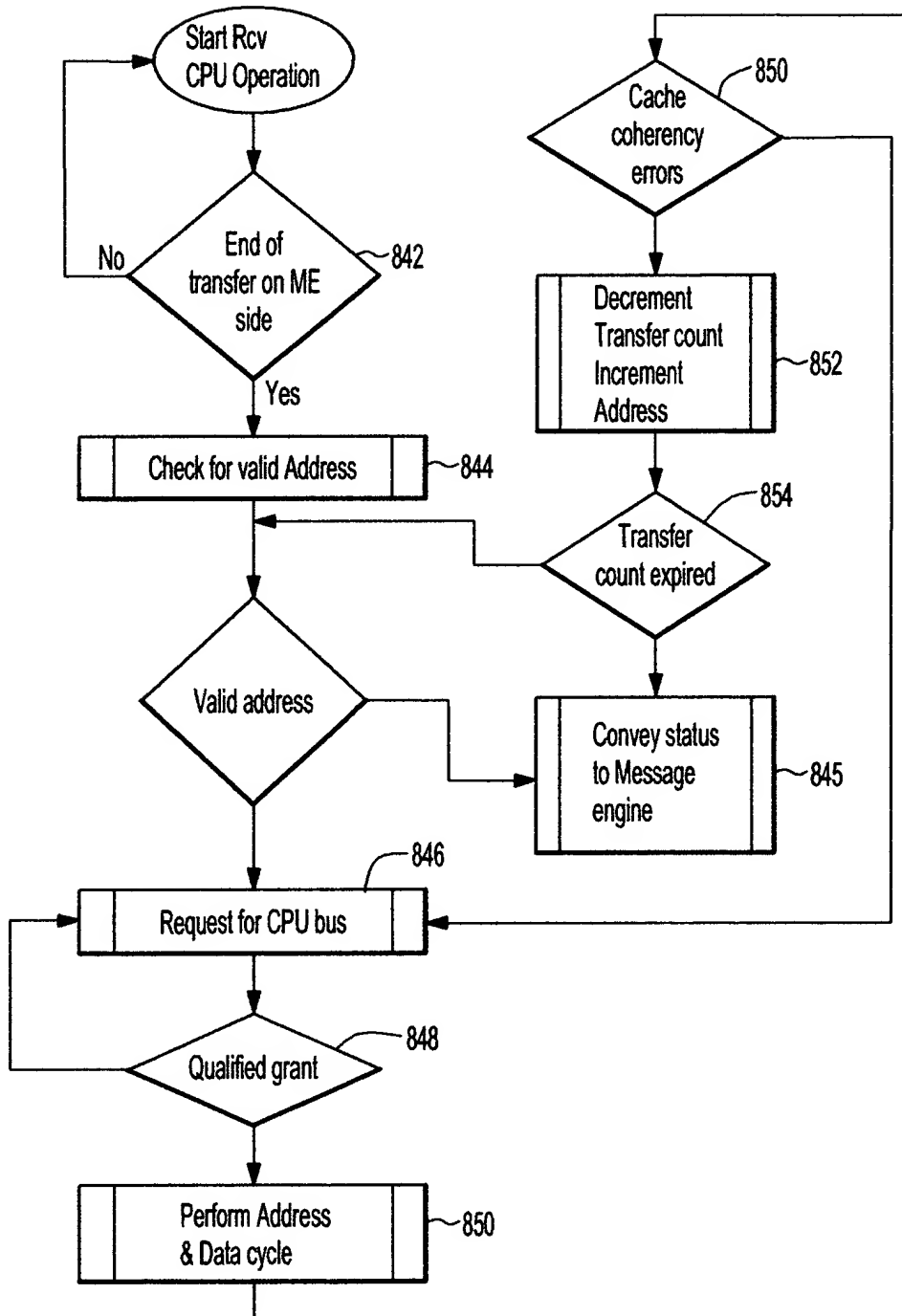


FIG. 15B